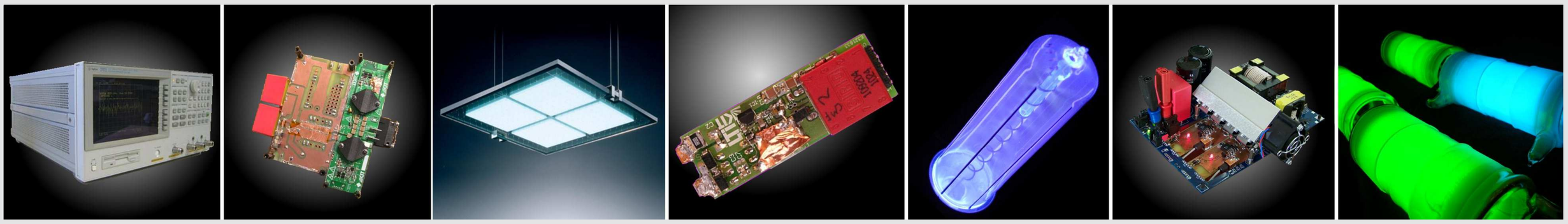
Karlsruhe Institute of Technology, KIT
Light Technology Institute ,LTI
Light and Plasma Technologies Group
Engesserstr. 13, 76131 Karlsruhe, Germany
www.lti.kit.edu

# Impedance Characterization of High-Frequency Gate Drive Circuits for Silicon RF MOSFET and Silicon-Carbide Field-Effect Transistors

**Michael Meisser**, Karsten Hähre

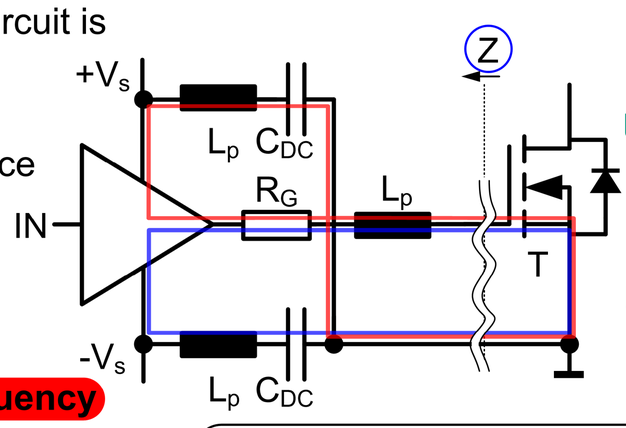
mail to: michael.meisser@kit.edu



## Multi-MHz Half-Bridges – Ensuring Necessary RF Switching Performance

**AC** — **evaluating gate drive performance** — **DC**

- because of parasitic inductance, RLC circuit is formed
- quality factor < 2 to prevent resonance




- low impedance **at operation frequency** for fast $C_{GS}$ charge

⇓

- use impedance spectrum measurement to characterize resonance behavior
- perform measurement under DC-bias

- static Voltage levels to be reached soon after switching
- low resistance **at DC** against Miller-feedback

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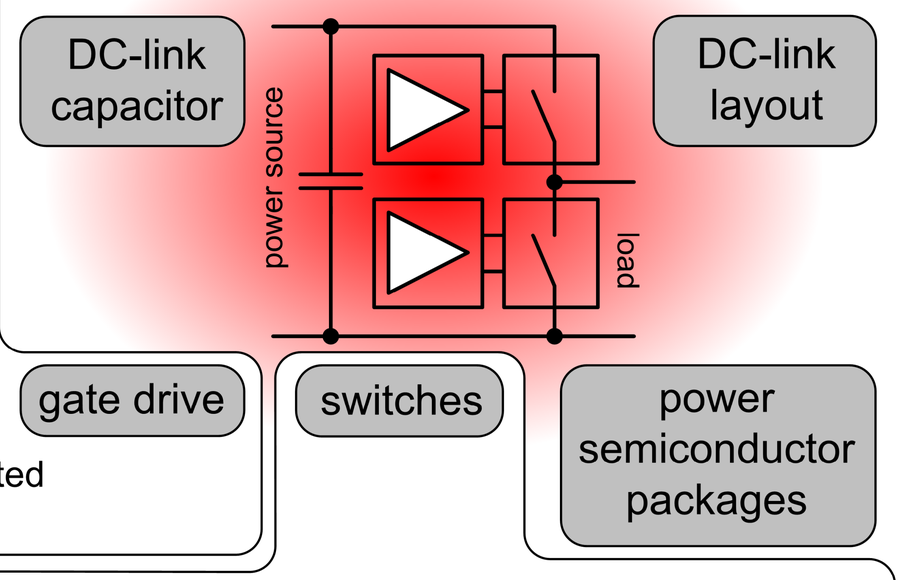
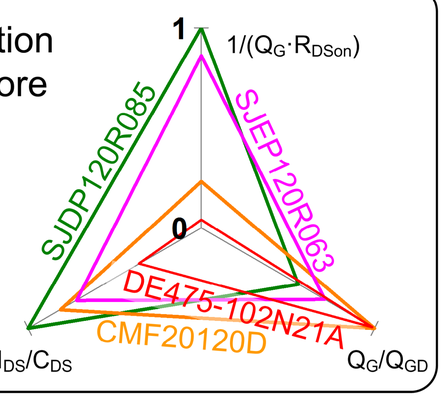
- maximum gate resistance value restricted

**critical circuit parts**

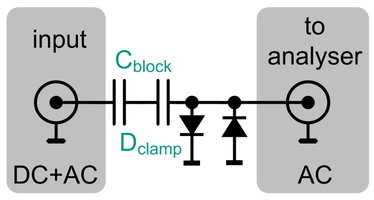



- Si and SiC MOSFETs offer high robustness needed for half-bridge configuration
- normally-on JFET is superior regarding FOM and maximum slew rate, therefore predestinated for HF-application

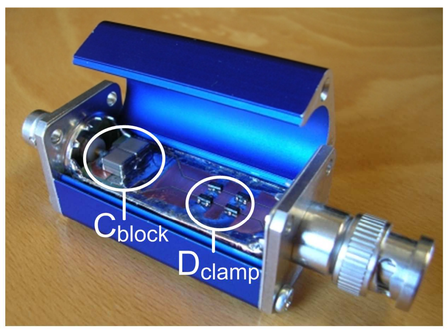
| device | type | $V_{GS}$ [V] | $I_{DS}$ [A] | FOM $1/(Q_G{*}R_{DSon})$ | robustness $Q_G/Q_{GD}$ | max. slew rate $I_{DS}/C_{DS}$ [V/ns] |
|---|---|---|---|---|---|---|
| DE475-102N21A | RF Si MOSFET | +15/ -15 | 24 | 0.015 | 2.078 | 120 |
| CMF20120D | SiC MOSFET | +25/ -5 | 24 | 0.085 | 2.107 | 275 |
| SJDP120R085 | SiC n-on JFET | +15(+3)/ -15 | 27 | 0.368 | 1.185 | 338 |
| SJEP120R063 | SiC n-off JFET | +15(+2)/ -15 | 30 | 0.317 | 1.502 | 244 |

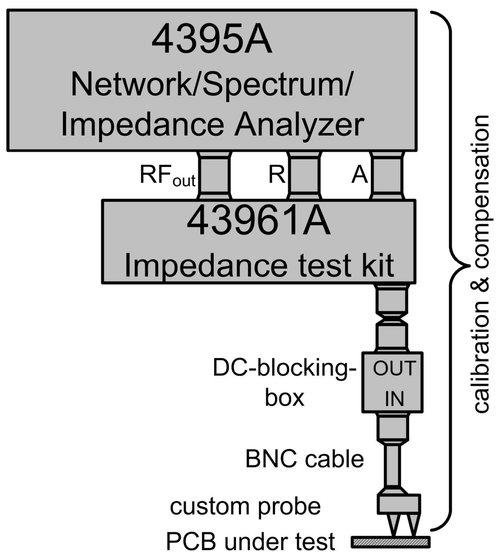



## Impedance Measurement under DC bias

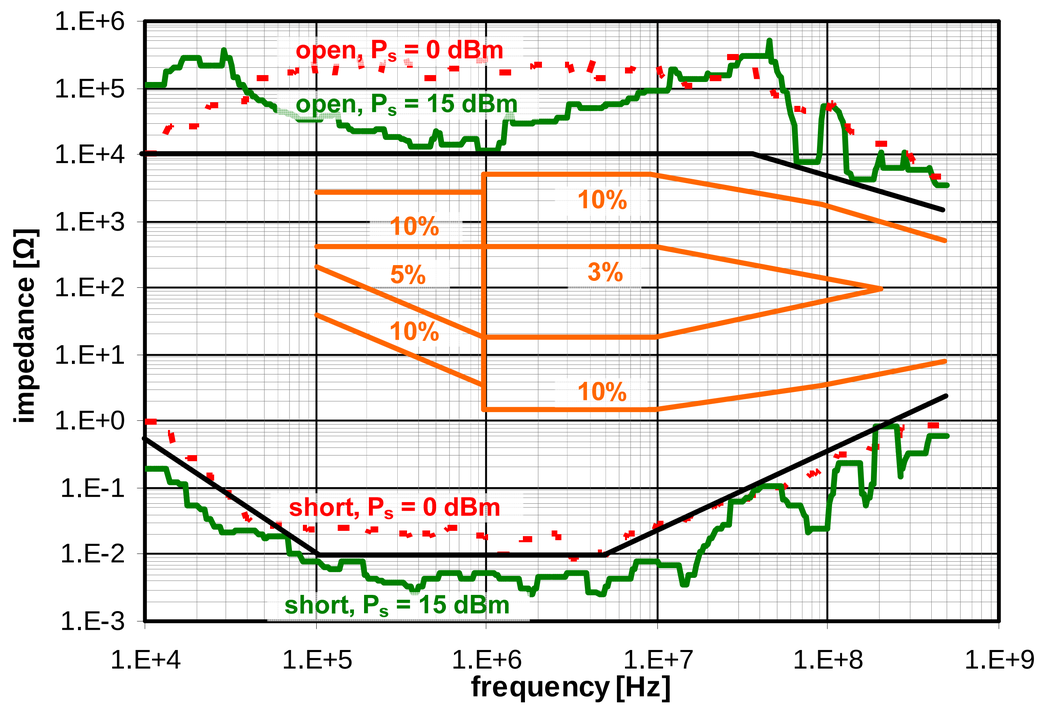



$C_{block}$ = NP0 MLCC 50 V 470 nF
4 parallel; $X_C$ @ 1 MHz = 13 Ω
$D_{clamp}$ = 4x antiparallel BAV74 Si RF diodes




## Measurement System Performance



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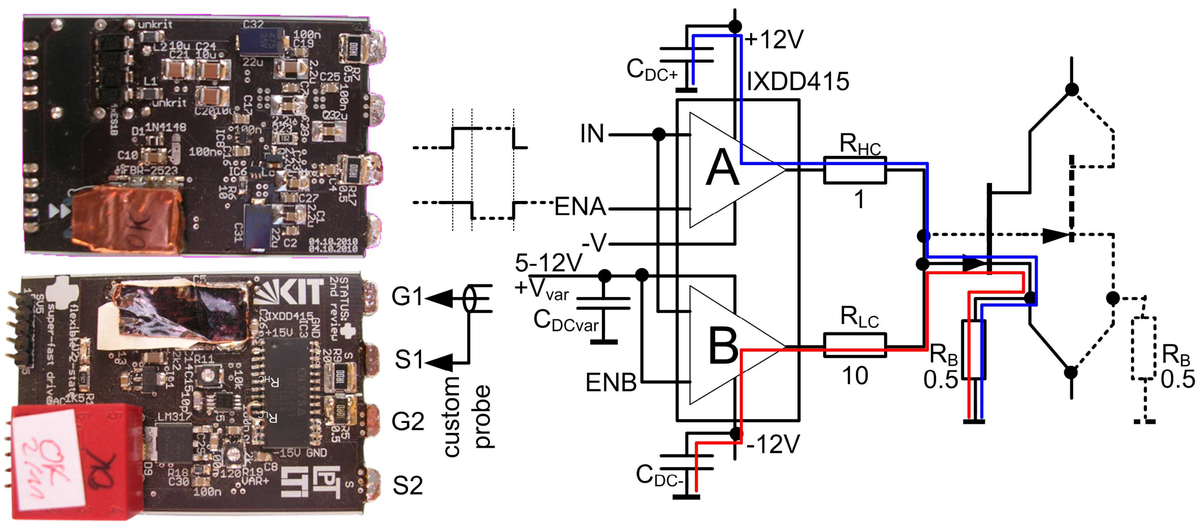
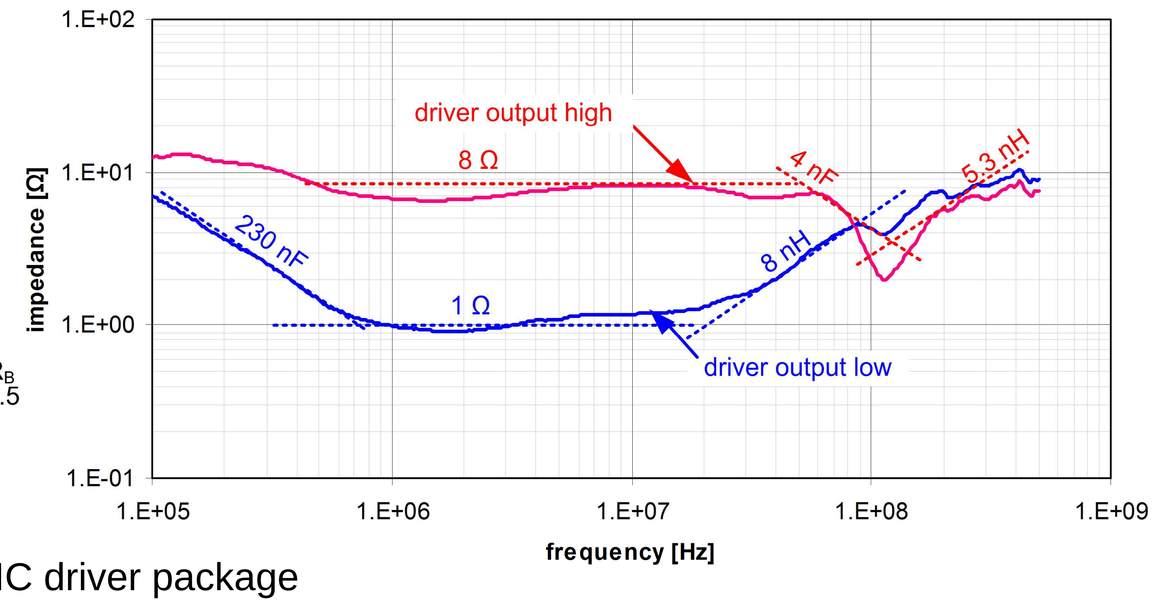
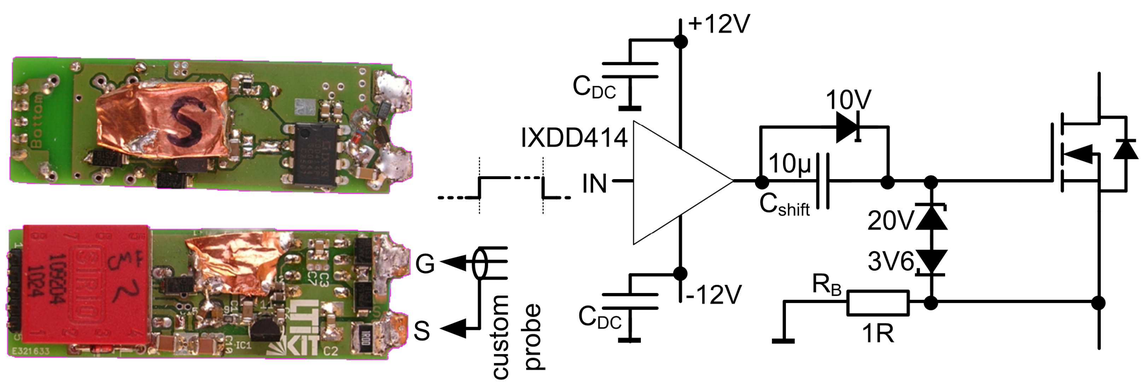
## SiC Normally-Off JFET Two-Current-Level Gate Driver Impedance Characterization

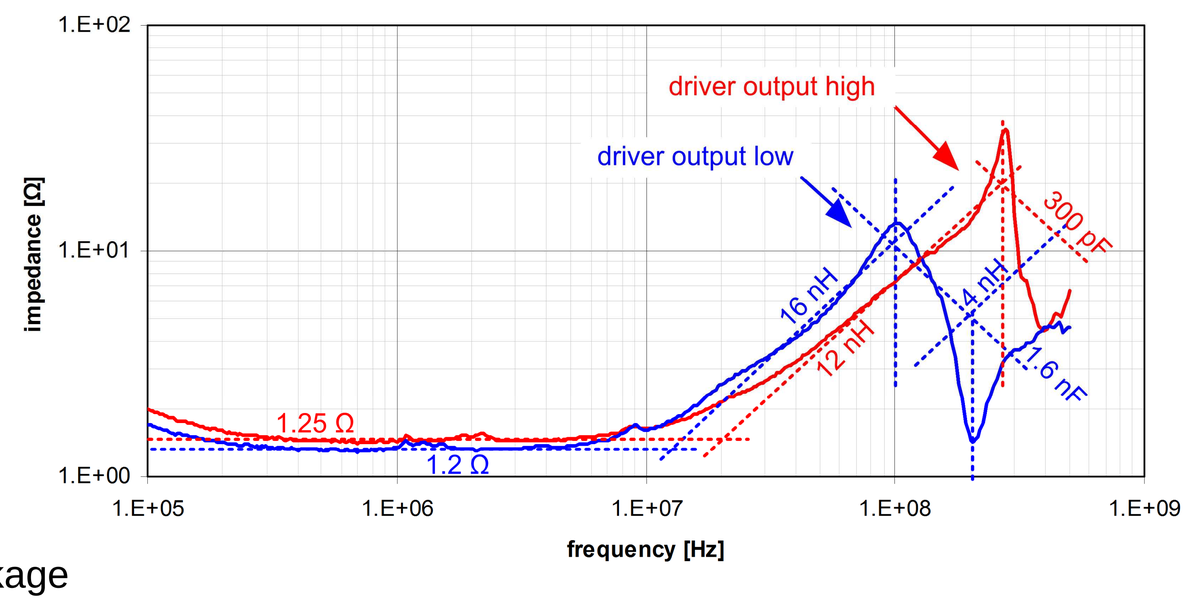



- comparatively low parasitic inductance due to RF-enhanced SOIC driver package
- different inductance values depending on current path
- too small DC bypass capacitor value

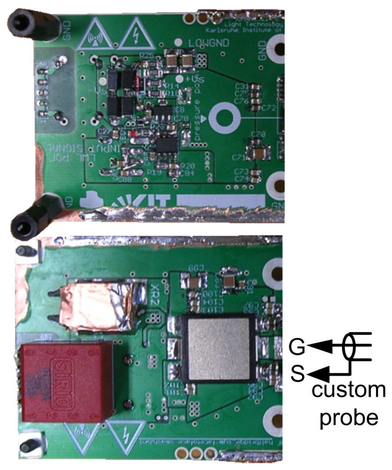
## SiC MOSFET Level-Shifting Gate Driver Impedance Characterization

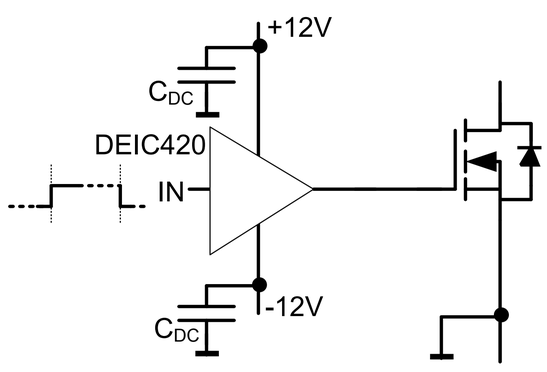


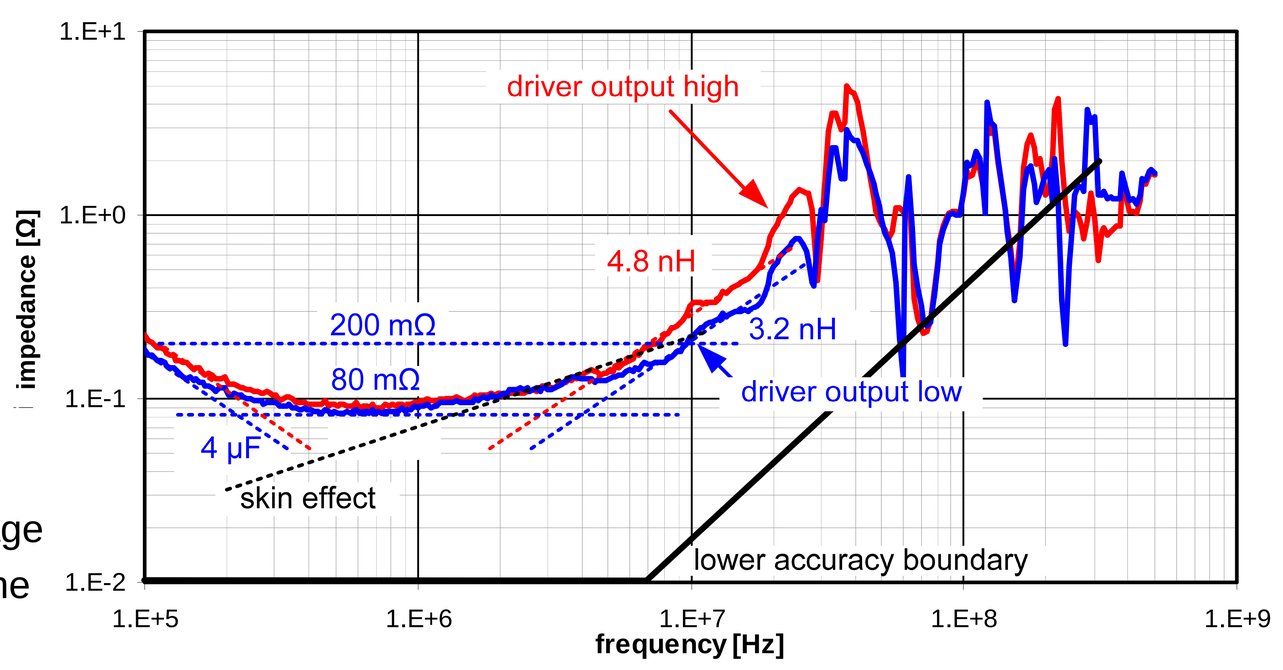




- comparatively high parasitic inductance due to DIP driver package
- sufficient DC bypass capacitor value ensures target impedance

## Si RF MOSFET Symmetrically Supplied Gate Driver Impedance Characterization




- lowest parasitic inductance due to DEIC-RF driver package
- the lower the target impedance, the higher the value of the necessary DC bypass capacitors ➡ paralleling